What is claimed is:

Sub #1

1. An integrated circuit comprising:

at least three cooperating frequency domains having variable operating frequencies;

cross-over logic to allow integral fractional ratio frequency domain cross-overs between more than one pair of frequency domains.

2. The integrated circuit of claim 1 wherein said cross-over logic is capable of providing at least sixteen different cross-over ratios.

3. The integrated circuit of claim 1 wherein said at least three cooperating frequency domains comprise:

a processor domain operable at a relatively large number of different frequencies;

a memory control domain;

a memory interface domain operable at a first relatively small number of frequencies, said first relatively small number being less than one-half of the relatively large number;

a bus interface domain operable at a second relatively small number of frequencies, said second relatively small number also being less than one-half the relatively large number.

4. The integrated circuit of claim 1 further comprising a mask generator circuit to compute and generate masking signals for said cross-over logic on the fly using selectable cross-over ratios.

Sub A1

5. An integrated circuit comprising:

a first portion operable at a first operating frequency chosen from a first plurality of frequencies;

a second portion operable at a second operating frequency chosen from a second plurality of frequencies, said second operating frequency being selectable to have at least two different mathematical relationships to said first operating frequency, said second portion to operate in cooperation with said first portion;

a third portion operable at a third operating frequency chosen from a third plurality of frequencies, said third plurality of frequencies and said first plurality of frequencies having at least some differing members, said third portion to operate in cooperation with at least one of said first portion and said second portion.

6. The integrated circuit of claim 5 wherein said first plurality of frequencies comprises a plurality of frequencies equal to the base frequency plus sequential integral multiples of an incremental frequency

7. The integrated circuit of claim 5 wherein said first portion is a processor portion, said

second portion comprises a graphics accelerator and memory interface logic, and said third portion comprises memory control logic.

Sub A1

8. The integrated circuit of claim 5 wherein said second operating frequency is an integral fraction of said first operating frequency.

9. The integrated circuit of claim 5 wherein said third portion is an external interface portion.

10. The integrated circuit of claim 9 further comprising a second external interface portion, said second external interface portion to cooperate with at least one of the first portion and the second portion and to operate at a different frequency than said at least one of the first portion and the second portion.

11. The integrated circuit of claim 5 further comprising:

a fourth portion operable at a fourth operating frequency, said fourth portion cooperating with said second portion, said fourth operating frequency being an integral fractional ratio of said second operating frequency for at least one of said second plurality of frequencies.

12. A system comprising:

an integrated circuit comprising:

a CPU portion to operate at a selectable first frequency which is one of a

first plurality of frequencies, said first plurality of frequencies being equal to a base frequency plus between zero and N times an incremental frequency;

a graphics portion to operate at a second frequency which is a function of the selectable first frequency;

a memory control portion to operate at said second frequency;

a memory interface portion to operate at a third frequency;

a bus interface portion to operate at a fourth frequency;

programmable cross-over logic to interface said bus interface portion and said memory interface portion to said memory control portion at selectable integral fractional clocking ratios;

a memory subsystem to communicate with said memory interface portion.

13. The system of claim 12 wherein said integrated circuit further comprises:

mask generation circuitry to compute and generate mask signals for said programmable cross-over logic.

14. An apparatus comprising:

a FIFO array comprising a plurality of storage elements to store data elements;

a plurality of writer assertion logic and reader response logic element pairs, one for each data element in said FIFO array;

a reader sequencer to maintain a reader FIFO pointer in a reader frequency

domain;

a plurality of reader status bits, each of said plurality of reader status bits corresponding one of said plurality of storage elements an element in said FIFO array;

a writer sequencer to maintain a writer FIFO pointer in a writer frequency domain;

a plurality of writer status bits, each of said plurality of writer status bits corresponding to one of said plurality of storage elements in said FIFO array.

Sub A1

15. The apparatus of claim 14 wherein each writer assertion logic and reader response logic element pair comprises:

writer assertion logic operable in said writer frequency domain to generate a first signal transition to indicate data is available, said first signal transition being either a positive transition or a negative transition, either of said positive transition and said negative transition indicating that said data is available;

reader response logic operable in said reader frequency domain to generate a second signal transition to indicate that said data has been received, said second signal transition being either the positive transition or the negative transition, either of said positive transition and said negative transition indicating that data has been received.

16. A clock domain cross-over apparatus comprising:

a plurality of latches to latch data items;

an array of status bits comprising one valid bit and one free bit for each of said plurality of latches;

writer logic to receive data into one of said plurality of latches and to toggle a writer indicator signal to cause a valid bit for that latch to be set;

reader logic to read data from one of said plurality of latches and to toggle a reader indicator signal to cause a free bit for that latch to be set;

masking circuitry to delay toggling on said writer indicator signal and said reader indicator signal to maintain setup times above a predetermined threshold.

17. The apparatus of claim 16 wherein said plurality of latches forms a FIFO array for data items and wherein said writer logic comprises a writer pointer and said reader logic comprises a reader pointer.

18. The apparatus of claim 17 wherein said writer logic is coupled to receive a writer half cycle signal to allow said writer logic to accept said reader indicator signal at half cycle points and wherein said reader logic is coupled to receive a reader half cycle signal to allow said reader logic to accept said writer indicator signal at half cycle points.

19. The apparatus of claim 16 wherein said reader logic comprises a reader set/reset latch

to generate said reader indicator signal and wherein said writer logic comprises a writer set/reset latch to generate said writer indicator signal.

Sub #1

20. The apparatus of claim 19 further comprising write live circuitry to bypass the writer set/reset latch to generate the writer indicator signal.

21. The apparatus of claim 16 wherein said masking circuitry comprises mask computation circuitry to compute from a selected frequency ratio when masks should be generated to maintain setup times above said predetermined threshold.

22. An integrated circuit comprising:

a first portion operable at a first plurality of frequencies, said first portion to operate in a first frequency domain;

a second portion operable at a second plurality of frequencies that are a ratio n/m to said first portion, said second portion to operate in a second frequency domain;

crossover logic between said first portion and said second portion, said crossover logic comprising:

a plurality of latches arranged as a FIFO array;

a plurality of status bits comprising:

a plurality of free bits;

a plurality of valid bits;

a writer element to maintain a write pointer to said FIFO array in said

first frequency domain;

a reader element to maintain a read pointer to said FIFO array in said second frequency domain;

domain crossing handshake circuitry to update said plurality of free bits and said plurality of valid bits.

Sub A1

23. The integrated circuit of claim 22 wherein said domain crossing handshake circuitry comprises:

writer assertion logic to toggle a writer indicator signal to either a first or a second logic value to indicate available write data;

reader response logic to receive said writer indicator signal and to indicate that valid data is available responsive to the writer indicator signal toggling to either the first or the second logic value;

reader assertion logic to toggle a reader indicator signal to either the first or the second logic value to indicate that a data item has been used;

writer response logic to receive said reader indicator signal and to indicate that a free FIFO entry is available responsive to the reader indicator signal toggling to either the first or the second logic value.

24. A mask generator comprising:

a writer clock N value input to receive an N value indicative of a first number of ticks for a first frequency domain;

a reader clock M value input to receive an M value indicative of a second

number of ticks for a target frequency domain;

a predetermined setup time indicator to indicate a minimum setup time, said minimum setup time being a minimum number of ticks;

mask signal generation circuitry to compute and generate a mask signal from programmable values of N and M to mask signal transitions that occur within said minimum number of ticks in said target frequency domain of a transition of a clock signal in said target frequency domain.

Sub A1

25. The mask generator of claim 24 wherein said predetermined setup time indicator is programmable to change the minimum setup time.

26. A method of transferring data from a first clock domain to a second clock domain, comprising:

storing a data item in a first entry in an array;

marking a free bit to indicate that said first entry is not free;

signaling the data item is available by toggling to any state a writer indicator;

continuing to receive data items in said array while free entries are available;

receiving said data item in said second clock domain;

signaling that the data item has been received by toggling to any state a reader indicator.

27. The method of claim 26 wherein signaling the data item is available comprises masking the writer indicator if less than a predetermined minimum setup time is

available.

28. The method of claim 26 further comprising:

maintaining a writer pointer in the first clock domain; and

maintaining a reader pointer in the second clock domain.

29. The method of claim 27 further comprising generating a masking signal by computing when said predetermined minimum setup time is available from the ratio M/N of clocks in the first clock domain and the second clock domain.